1. (currently amended) A high electron mobility transistor (HEMT) comprising:

a channel layer being composed of a II-VI compound semiconductor zinc oxide **(ZnO)**;

a gate contact disposed in proximity to, but not in contact with, said channel layer; and

a gate insulating layer disposed between and in contact with said gate contact and said channel layer and composed of at least one of a Group-III nitride compound semiconductor and a magnesium zinc oxide (MgZnO) quantum well structure, said gate insulating layer having side walls, said gate contact positioned between the sidewalls of said gate insulating layer so that sides of said gate contact face the side walls of said gate insulating layer.

2. (previously presented) A HEMT according to claim 1 wherein said gate insulating layer is composed of at least one of an epitaxially grown Group-III nitride compound semiconductor and a MgZnO quantum well structure.

3. (original) A HEMT according to claim 2 wherein said channel layer is composed of an epitaxially grown Group-II-VI zinc oxide compound semiconductor.

4. (previously presented) A HEMT according to claim 1 wherein said gate insulating layer is composed of a Group-III compound semiconductor expressed by a chemical formula $Al_xGa_{1-x}N$ ($0.3< x \leq 1$) or $Mg_xZn_{1-x}O$ ($0.1< x <.4$).

5. (previously presented) A HEMT according to claim 1 wherein said channel layer is formed on a substrate comprising at least one of zinc oxide (ZnO), silicon carbide (SiC), sapphire ($Al_2O_3$), and silicon (Si) and has a bulk resistivity higher than $10^5$ ohm-centimeter ( $\Omega$-cm).

6. (previously presented) A HEMT according to claim 1 wherein the thickness of said gate insulating layer ranges from 0.30 nanometer (nm) to 50 nm.

7. (previously presented) A HEMT according to claim 1 wherein said HEMT employs piezoelectric doping created by strain due to lattice mismatch between the channel layer and the gate insulating layer that produces a two-dimensional electron gas (2DEG) near an interface between the channel layer and the gate insulating layer to avoid usage of a conventional doping method.

8. (original) A HEMT according to claim 1 wherein said gate contact is selected from the group consisting of titanium (Ti), platinum (Pt), silver (Ag), gold (Au), chromium (Cr), alloys of titanium(Ti) and tungsten (W), and platinum silicide (PtSi).

9. (previously presented) A HEMT according to claim 1 wherein source and drain contacts to said channel layer comprise an alloy of titanium (Ti), silicon (Si), aluminum (Al) and nickel (Ni).

10. (previously presented) A HEMT according to claim 1 and further comprising a passivation layer on said gate contact and said source and drain contacts to said channel layer.

11. (canceled)

12. (previously presented) A HEMT according to claim 1 wherein an area of said gate contact with said gate insulating layer is decreased due to the presence of said sidewalls.

13. (previously presented) A HEMT according to claim 1 wherein the channel layer is composed of ZnO and is grown by metal organic chemical vapor deposition (MOCVD).

14. (currently amended) A HEMT according to claim 1 wherein gate insulating layer is grown by metal organic chemical vapor deposition (MOCVD) and sequentially laminated on said channel layer, **the HEMT further comprising:**

**a substrate composed of ZnO, the channel layer laminated onto the substrate**[[and the channel layer in turn is laminated onto a substrate, said channel layer and said substrate composed of ZnO]].

15. (previously presented) A HEMT according to claim 14 wherein the substrate is a c-surface substrate.

16. (canceled)

17. (currently amended) A method comprising the steps of:

defining a channel layer composed of a II-VI compound semiconductor zinc oxide **(ZnO)**;

forming a gate insulating layer in contact with said channel layer and composed of at least one of a Group-III nitride compound semiconductor and a magnesium zinc oxide (MgZnO) quantum well structure, said gate insulating layer formed with side walls; and

forming a gate contact disposed on and in contact with said gate insulating layer and positioned between said side walls, said gate contact formed to have sides facing said side walls of said gate insulating layer, said gate contact formed in proximity to, but not in contact with, said channel layer.

18. (previously presented) A method according to claim 17 wherein the gate insulating layer is formed by metal organic chemical vapor deposition (MOCVD).

19. (previously presented) A method according to claim 17 wherein the channel layer is formed on a c-surface ZnO substrate.

20. (canceled)